THIN-FILM INTRACORTICAL RECORDING MICROELECTRODES

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Center for Wireless Integrated MicroSystems
Department of Electrical Engineering and Computer Science
The University of Michigan
Ann Arbor, Michigan
48109-2122

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Thin-Film Intracortical Recording Microelectrodes

Summary

During the past quarter, we have continued to distribute passive probes built with technology developed under these contracts to investigators nationwide. Nearly 5000 probes have now been provided, resulting in over 180 publications and presentations. A new mask set is now in preparation for fabrication this fall.

The first soak tests of active probes also began last quarter. The test vehicle was a 32-site front-end selected and buffered probe that also contained a number of test structures, including test transistors. The probe circuitry was encapsulated with LTO, which in some cases was covered by sputtered or electroplated gold shields. For probes operated at body temperature, the primary change noted was an increase in gate current for the test transistors; for probes soaked at 70°C, the bonding pads failed early in the tests. There was no observed degradation of the interconnect on the probes, however. At this point it is not known where the shift in the gate currents is an on-chip change or whether it is associated with the leads from these devices. We suspect the latter. In a second series of tests with an improved lead structure, the probes have been functioning for over a week with no noted changes at body temperature. Probes with integrated ribbon cables will be tested during the coming quarter.

We have now performed additional tests on the capacitively-coupled amplifiers developed for the probes, correcting earlier measurements of their associated noise. The amplifiers have an input-referred noise of 16.6μVrms (10Hz – 10kHz). For the site, input selector, and amplifier together, the noise is 19.2μVrms. We have iterated the amplifier design to reduce its noise to 7.2μVrms. The amplifiers provide a gain of 38.2dB with a power-supply-rejection-ratio of 50.5dB. The output offset voltage is –45mV, which is adequate for the succeeding multiplexers. On-platform spike detection circuitry is being designed with a 5b successive approximation converter. The ADC has a maximum bandwidth of 400kHz and dissipates 330μV from ±1.5V supplies.

We are also in the final stages of designing a wireless interface to the recording probes. The chip being characterized includes all of the front-end circuitry for the probes along with the on-chip transmitter. This transmitter is presently being characterized at a carrier frequency of 49MHz, where it allows bit rates of 1.6Mbps and dissipates 1.7mW from 3.3V. The on-chip voltage regulators produce 1.7V and 3.4V outputs with line regulation better than 3mV/V and load regulation better than 2mV/mA. The power-on-reset circuitry produces a reset pulse width of 290μsec. The front-end circuitry is fully functional with an overall dissipation of about 480μW from 7V. A 10b ADC is being designed for use with analog output probes. It dissipates 1.27mW at a cycle time of 4μsec. The front-end control logic verifies the input commands received using a Manchester encoder and formats the received commands/data for use by the probes. The last of these circuit blocks are now ready for fabrication. We hope to operate the entire probe system wirelessly by the end of the year.

Thin-Film Intracortical Recording Microelectrodes

1. Introduction

The goal of this program is the realization of batch-fabricated recording electrode arrays capable of accurately sampling single-unit neural activity throughout of volume of cortical tissue on a chronic basis. Such arrays will constitute an important advance in instrumentation for the study of information processing in neural structures and should be valuable for a number of next-generation closed-loop neural prostheses, where stimuli must be conditioned on the response of the physiological system.

The approach taken in this research involves the use of solid-state process technology to realize probes in which a precisely-etched silicon substrate supports an array of thin-film conductors insulated above and below by deposited dielectrics. Openings in the dielectrics, produced using photolithography, form recording sites which permit recording from single neurons on a highly-selective basis. The fabrication processes for both passive and active (containing signal-processing circuitry) probe structures have been reported in the past along with scaling limits and the results of numerous acute experiments using passive probes in animals. In moving to chronic implant applications, the major problems are associated with the preserving the viability of the sites in-vivo (preventing tissue encapsulation of the sites) and with the probe output leads, both in terms of their number and their insulation. The probe must float in the tissue with minimal tethering forces, limiting the number of leads to a few at most. The encapsulation of these leads must offer adequate protection for the megohm impedance levels of the sites while maintaining mechanical lead flexibility.

Our solution to the lead problem has involved two steps. The first has been to embed circuitry in the probe substrate to amplify and buffer the signals and to multiplex them onto a common output line. Using this approach, signal levels are increased by factors of over 100, impedance levels are reduced by three to four orders of magnitude, and the probe requires only a few leads for operation, independent of the number of recording sites. A high-yield merged process permitting the integration of CMOS circuitry on the probe has been developed, and this circuitry has been designed and characterized. The second step has involved the development of silicon-based ribbon cables, realized using the same probe technology, to conduct the neural signals to the outside world. These cables have shown significant advantages over discrete leads, both in terms of the ease with which chronic implants can be assembled and in terms of the ability of the cables to survive long-term biased soaks in saline. The cables can be built directly into the probes so that they come off of the wafer as a single unit, requiring no joining or bonding operations between them. The cables are also significantly more flexible than previously-used discrete wire interconnects.

This contract calls for the development of active probes for neural recording. A 64-site 8-channel probe with site selection and signal buffering but no multiplexing has

been developed (PIA-2B) along with a high-end multiplexed probe that includes gain (PIA-2). These probes are now being refined and applied to in-vivo applications. Investigations are on-going to better understand site encapsulation, which limits the lifetime of chronic recording structures, and telemetry is being developed to allow the probes to be operated over a wireless link, eliminating the percutaneous connector.

During the past quarter, we have continued to distribute probes to a growing number of users nationwide. We have begun soak tests on active probes in-vitro and in-vivo. We are also completing work on platform-mounted spike recognition circuitry for the probes as well as a wireless interface for them. Work in these areas is discussed in the sections below.

2. Passive Probe Developments

Passive probes based on NPP technology continue to be distributed to investigators in the U.S. and abroad through the Center for Neural Communication Technology (CNCT). Nearly 5000 probes have been shipped since distribution began in 1988. This effort has resulted in over 180 publications and presentations (see www.engin.umich.edu/facility/cnct/papers.html for complete list).

In addition to distributing standard designs from a passive probe catalog, the CNCT offers a custom design service to advanced probe users and collaborators. We are currently in the design phase of the CNCT6 mask set. Designs on this mask set include cortical recording probes for Daryl Kipke and Justin Williams of the University of Michigan, a probe for stimulation of cochlear nucleus for Douglas McCreery of Huntington Medical Research Institutes, a recording probe for inferior colliculus for Bryan Pfingst of the University of Michigan, a spinal cord recording probe for Mesut Sahin of Louisiana Tech University, and a probe for culturing neurons for Bradford Orr of the University of Michigan. Fabrication will occur in the coming quarter.

3. Soak Testing of Active Probes

Animal experiments have shown that passive neural probes encapsulated with an oxide/nitride/oxide dielectric stack show no signs of failure and can record successfully for a year or longer. Soak tests with passive probes encapsulated with electroplated gold suggest that these packages remain hermetic at body temperature for many decades. However, little work has been done to characterize the chronic in-vivo performance of active probes. The few active probes tested in-vivo in the past indicated that active probes encapsulated only with low temperature oxide (LTO) and under power (i.e., voltage biased) have an expected lifetime of only several hours in vivo but the reasons for failure were not clear.

In order to determine the lifetime of active recording neural probes and identify likely failure modes, an active probe was designed for chronic in-vitro soak tests and in-

vivo implants. This probe, shown in Fig. 1, has thirty-two recording sites which are front-end-selected and buffered onto four output channels. Test structures to monitor the

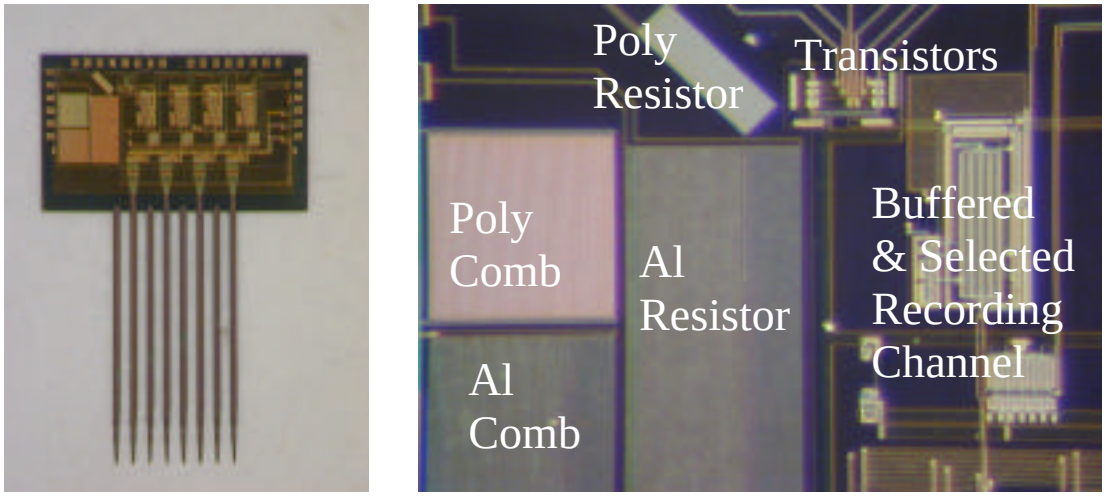

Fig.1: Fully fabricated probe designed for chronic implantation in guinea pig auditory cortex, left. Detail of test circuitry, at right.

integrity of the polysilicon and aluminum interconnect are also present. Transistors with bonding pads connected to source, gate, and drain are included in order to test the correct functioning of the devices during implantation and to monitor for evidence of gate damage or other device failure. Versions of this probe with and without a sputtered gold circuit shield, as well as a version with a thick (2-3 μm) electroplated gold shield, have been fabricated.

An initial round of soak tests involving five probes has been carried out for a period of fifteen weeks. Probes with a sputtered gold circuit shield were used for these tests. The probes were fastened with epoxy to a metallic chip carrier and wire bonded with gold wire, which in the past has proven to be reasonably resistant to corrosion. The chip carrier was then immersed in phosphate-buffered saline (PBS) in a sealed glass jar fitted with a pressure relief valve, and placed on a temperature-controlled hotplate. The temperature for three of the probes was 37°C, and for three it was 70°C. One of the probes in the 70°C broke during handling and had to be removed from the experiment. The packages were periodically removed from saline, rinsed thoroughly in DI water, dried and tested. The results are summarized in Table 1, below. For the body temperature group, the primary change observed was a significant increase in the amount of current flowing into the test transistor gates. For the higher temperature group, failure of the adhesion of several of the gold bonding pads was observed relatively early in the soaks, at which point further electrical testing of the transistors was impossible. It was possible to monitor the interconnect test structures, however, and this was continued until the

termination of the experiment after 15 weeks. In none of the five probes was failure of either the polysilicon or aluminum interconnect observed during this time. Prior to this experiment, etching of the aluminum interconnect was the expected failure mode for the probes. A shift in transistor thresholds was observed, with no clear trend in the magnitude or even direction of the shifts seen.

Device Name	**Temperature**	**Duration (time to failure)**	**Observed Failure Mode**	**Comments**
NIH-A1-4-1	-	-	-	Broken during handling.
NIH-A1-4-2	37°C	4 days	Gate leakage?	No sign of poly or Al interconnect failure (no change in resistance) for 15 weeks.
NIH-A1-4-3	37°C	14 days	Gate leakage?	No poly/Al interconnect failure, 15 weeks
NIH-A1-4-4	37°C	11 days	Gate leakage?	No poly/Al interconnect failure, 15 weeks
NIH-A1-4-5	70°C	19 hrs	Bond pad adhesion failure	No poly/Al interconnect failure, 15 weeks
NIH-A1-4-6	70°C	51 hrs	Bond pad adhesion failure	No poly/Al interconnect failure, 15 weeks.

Table 1: Summary of Active Probe Soak Test Results.

It is difficult to say at this point whether the observed gate currents are due to leakage within the transistor gates, or to some mechanism of encapsulation failure that is causing current to flow from the gate input line to somewhere else on or off the probe. An example of a gate voltage versus current curve is given in Fig. 3. The x-axis is formatted such that the gate voltage is plotted as the difference between Vss (5 volts) and the gate voltage, and we can see that for both the PMOS and NMOS devices, the curve appears to be that of a diode which turns on as the gate is biased 1.5 volts or so away from Vss. That is, there appears to be a non-ohmic short between the positive power supply and the gate. Whether or not this “short” is intrinsic to the probe or is related to a breakdown in probe encapsulation (i.e. in the package itself, the bondwires and/or bondpad insulation) will be the subject of a future investigation with a version of the probe with an integrated ribbon cable, as described below.

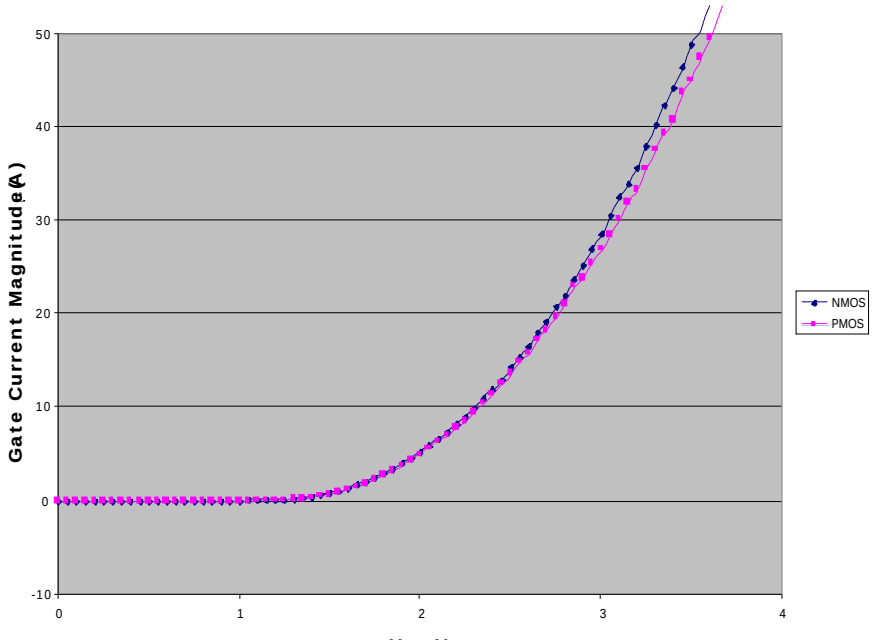

Fig. 2: IV curve for test transistors on device NIH-A1-4-4 after approximately four weeks of immersion, showing significant gate leakage.

In the current set-up the gold wire bonds were exposed to saline, so it was not possible to test the overall recording capability of the probe or to voltage-bias the circuitry during immersion. In order to address this shortcoming, a second series of soak tests is underway. This round of tests uses probes that are packaged on a PC board stalk. The wire bonds and a portion of the stalk are encapsulated with medical grade silastic, and the stalk is passed through a hole in a threaded glass jar fitted with a pressure relief valve. The hole is sealed with plumber's putty, which allows the probe to be periodically removed for testing. Because there are electrical feedthroughs, and because the wire bonds are sealed in silastic and thus encapsulated, it is possible to test the probe while immersed and to bias the circuitry continuously. The first such probe has been under continuous 5V bias at 37°C and has been recording successfully for just over a week.

In addition to providing the ability to continuously bias the probe, and to provide feedback about the probe recording ability, it is hoped that the use of the silastic-encapsulated PC board instead of a bare chip carrier will provide better (off-chip) interconnect isolation and provide a clue as to whether the previously observed gate leakage is intrinsic to the probe. In order to fully answer this question, a version of the same probe has been designed with a silicon ribbon cable. This design is similar to one that has been successfully used in guinea pig and rat cortex to record for up to one year. This probe has been fabricated, packaged, and tested (Fig. 3), representing the first time that a probe with active circuitry has made with an integrated ribbon cable. Soak tests with this probe will be carried out in the next quarter; in addition it is hoped to carry out chronic in-vivo testing of the device in the near future.

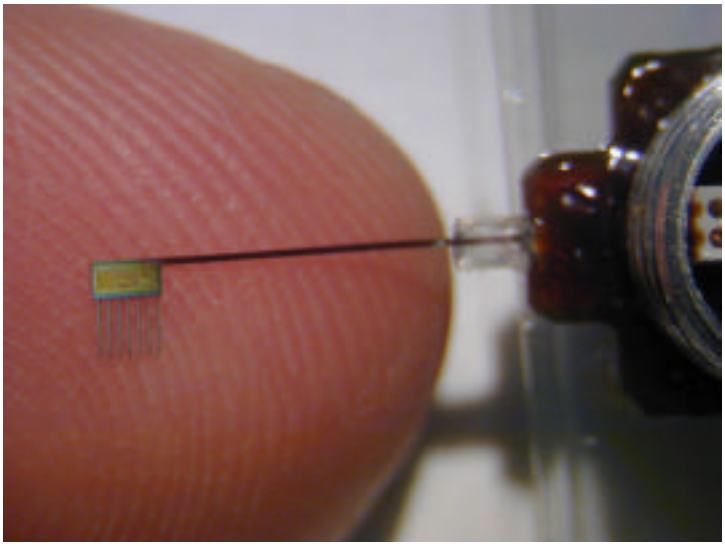

Fig. 3: Probe with integrated ribbon cable for chronic implantation and soak testing. Circuitry is identical to that shown in Fig. 1.

4. Development of On-Platform Signal Processing for Chronic Recording Probes

During the past quarter additional measurements have been completed on the capacitively-coupled amplifier (Fig. 4) and improvements have been made were necessary for the upcoming active probe run scheduled for late summer 2002. The input referred noise of the amplifier has been re-analyzed since the last quarterly report, where the integration of the noise was incorrect due to an invalid assumption. In order to obtain a more accurate integration of the input referred noise, the measured noise power of the amplifier was entered into EXCEL and a curve fit was done as shown in Fig. 5. The accuracy of the curve fit is determined by R^2 in Fig. 5, with a perfect fit yielding an R^2 value of 1. The equation generated by EXCEL was very accurate as indicated by the R^2 value shown. This equation was then integrated from 100Hz to 10kHz using Matlab, resulting in an input referred noise for the amplifier of $16.6\mu V_{rms}$. The same procedure was preformed for the noise of the site, front-end selector, and pre-amplifier in grounded saline as shown in Fig. 6. This yielded a total integrated input referred noise (100Hz-10kHz) for the $100^2\mu m$ iridium recording site, front-end selector and pre-amplifier of $19.2\mu V_{rms}$. The noise data for both the pre-amplifier alone and the site, front-end selector, and amplifier in grounded saline are shown in Fig. 7.

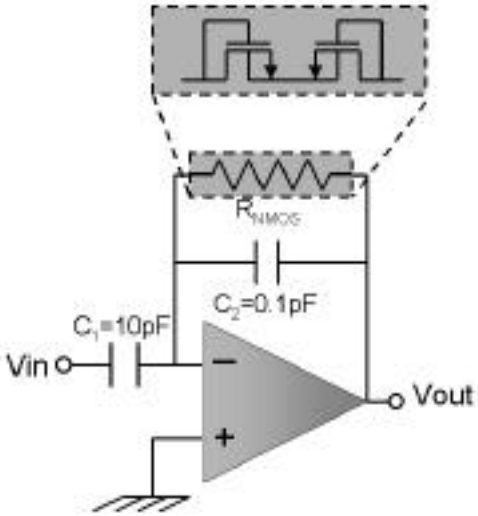

Fig. 4: Capacitively-Coupled Pre-amplifier

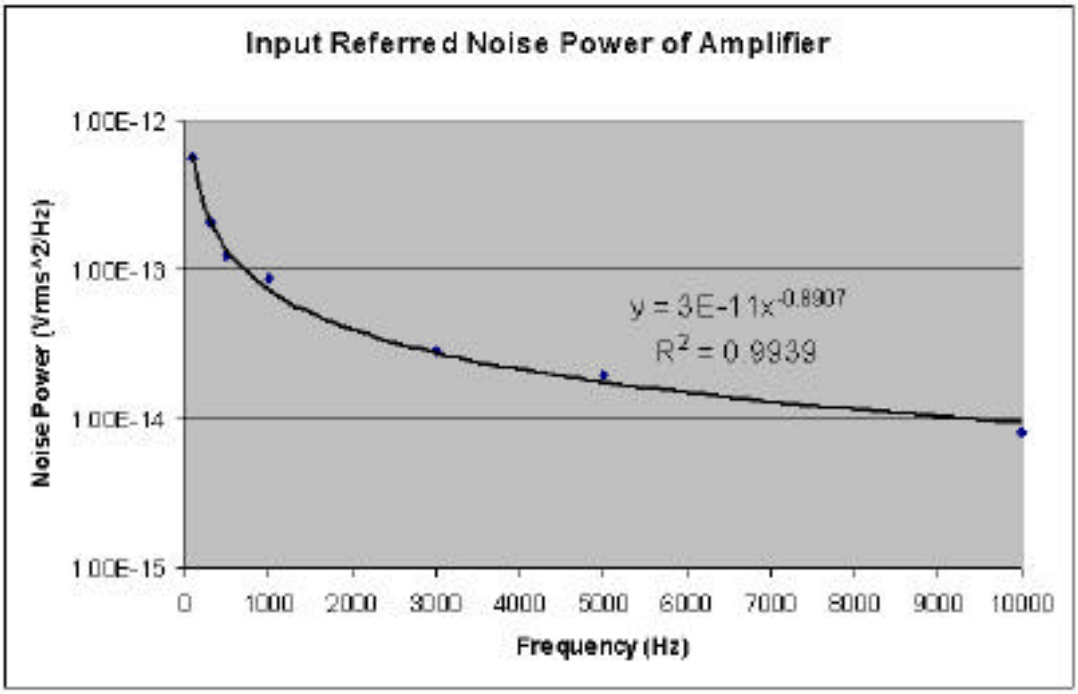

Fig. 5: Input Referred Noise Power and Curve Fit Data for Pre-amplifier

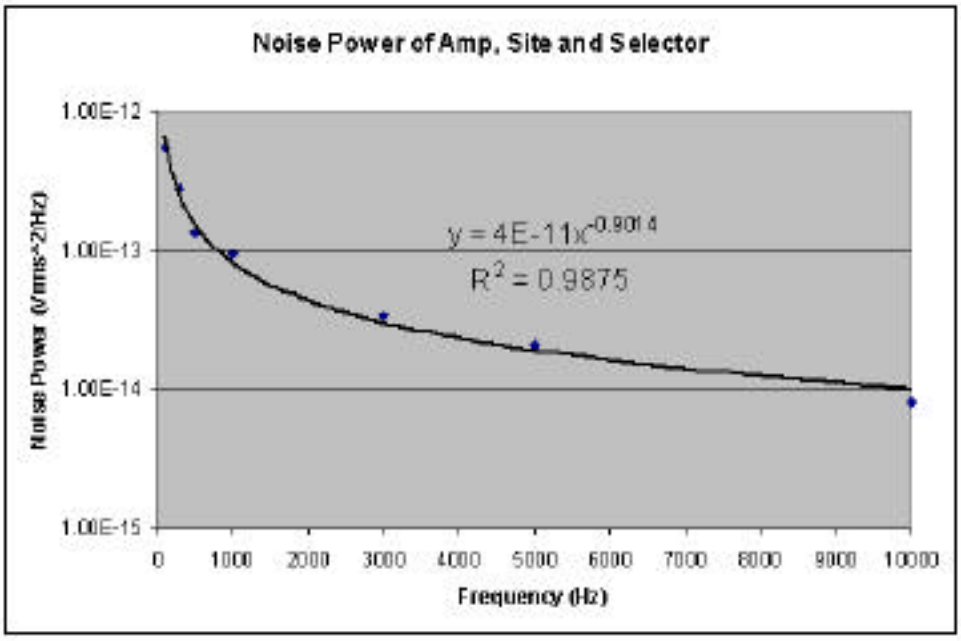

Fig. 6. Input Referred Noise Power and Curve Fit Data for Site, Front-end Selector and Pre-amplifier

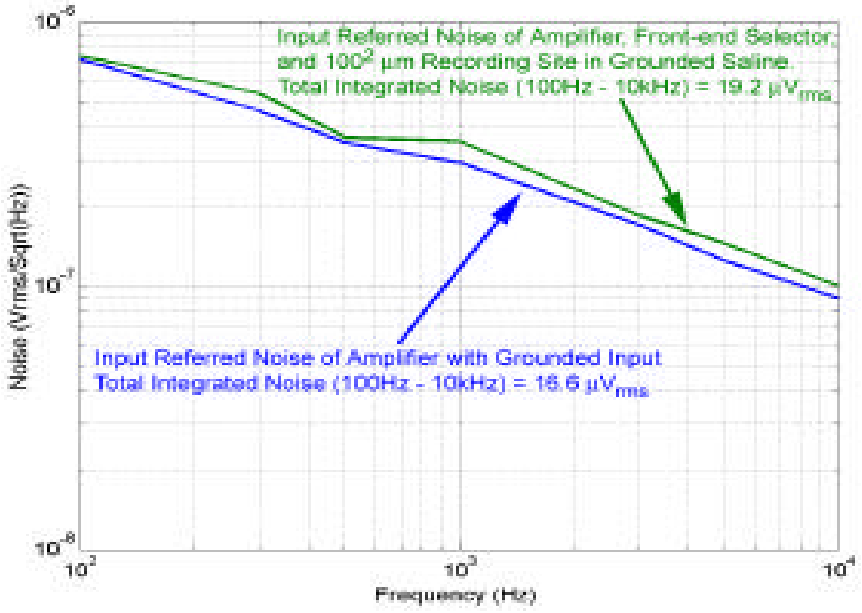

Fig. 7: Measured Input Referred Noise of Amplifier Alone and Amplifier, Front-end Selector and Site in Grounded Saline

Using the data measured from the pre-amplifier the flicker noise coefficients, $KF_{nmos}=40x10^{-25}$ (V^2F) and Kf_{pmos} = $20x10^{-25}$ (V^2F) have been modeled for our 3μm CMOS process. In addition, the flicker noise exponential for our process, AF = 0.9, has been extracted from the measured data. Using these updated parameters, the input differential pair and active load of the pre-amplifier have been enlarged to reduce the integrated input referred noise to 7.2μV_{rms} from 100Hz to 10kHz, Fig. 8.

Since PIA-2 is designed to operate over the wireless telemetry link currently under development, the gain of the on-chip amplifier was measured versus supply voltage as shown in Fig. 9. The closed loop gain of the amplifier is constant even for large deviations in supply voltage. The measured PSRR of the amplifier is 50.5dB at 1kHz, which is adequate to reject digital noise on the supply, while the 4MHz supply ripple is well outside the in-band gain on the amplifier.

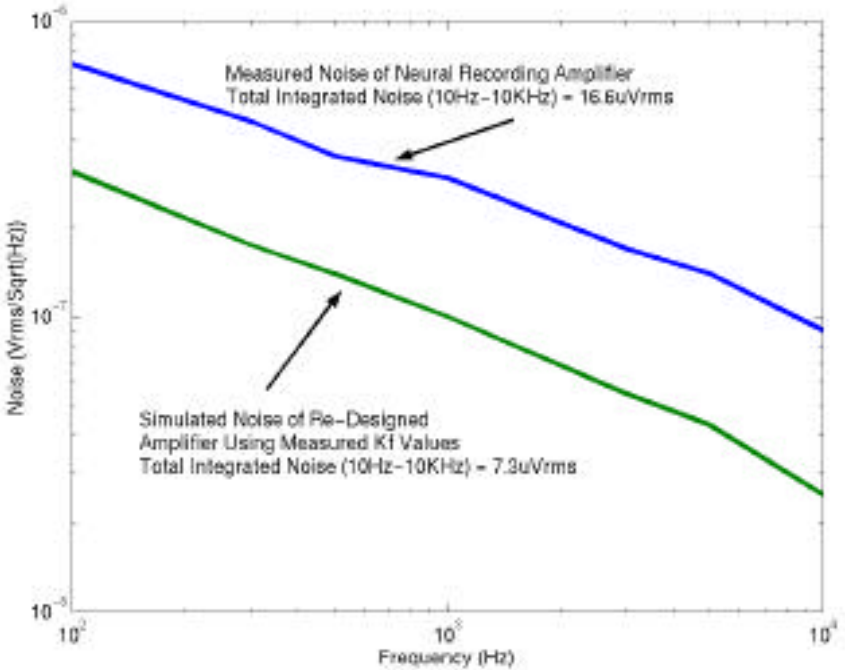

Fig. 8: Measured Input Referred Noise of Pre-amplifier and Simulated Noise of R designed Amplifier using extracted KF and AF values

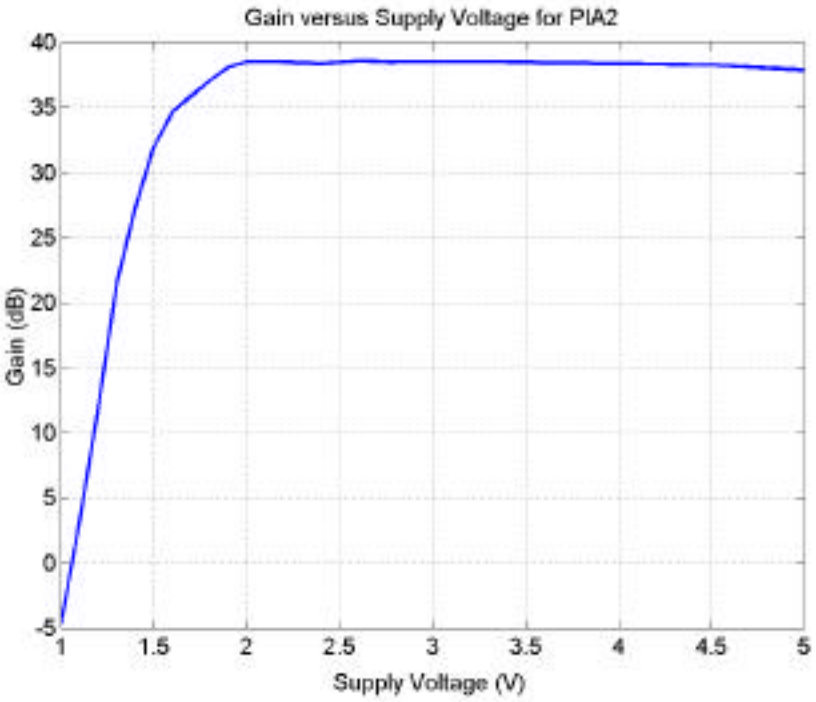

Fig. 9: Amplifier Gain vs. Supply Voltage

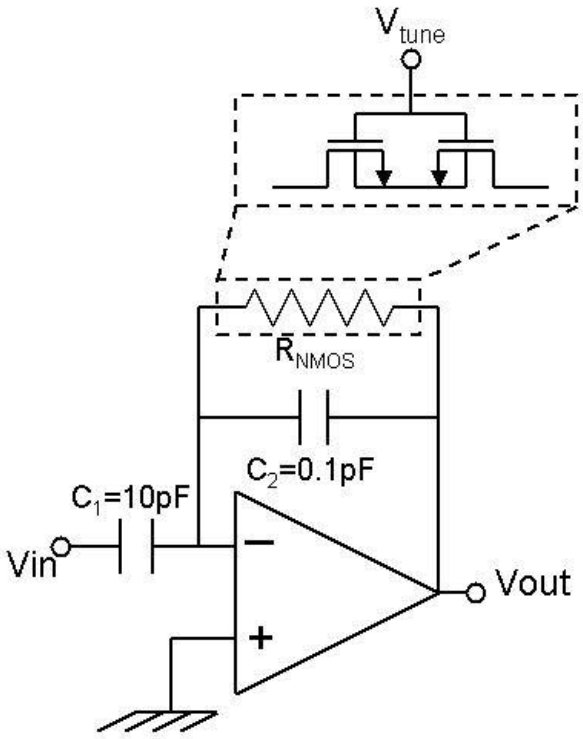

Fig. 10: Tunable Capacitively-Coupled Neural Recording Amplifier

Two of the main advantages of the capacitively-coupled amplifier are the stable, repeatable gain and the low output offset voltage. The output offset voltage measured across 20 amplifiers on 4 separate probes had a mean value of -45mV with a standard deviation of 25mV. The mean gain of the amplifier measured across 20 channels on four probes was 38.2dB with a standard deviation of 0.45dB. The gate to source capacitors of the sub-threshold NMOS transistors in Fig. 4 shunt C2, causing a reduction in gain. Since the gate oxide thickness does not track with the capacitor oxide thickness, these capacitors also introduce variance into the gain. To eliminate this problem, the gates of the feedback transistors can be brought out to a pad as shown in Fig. 10. This will also allow the low frequency cut-off of the amplifier to be tuned for recording both field potentials and single unit activity (Fig. 11).

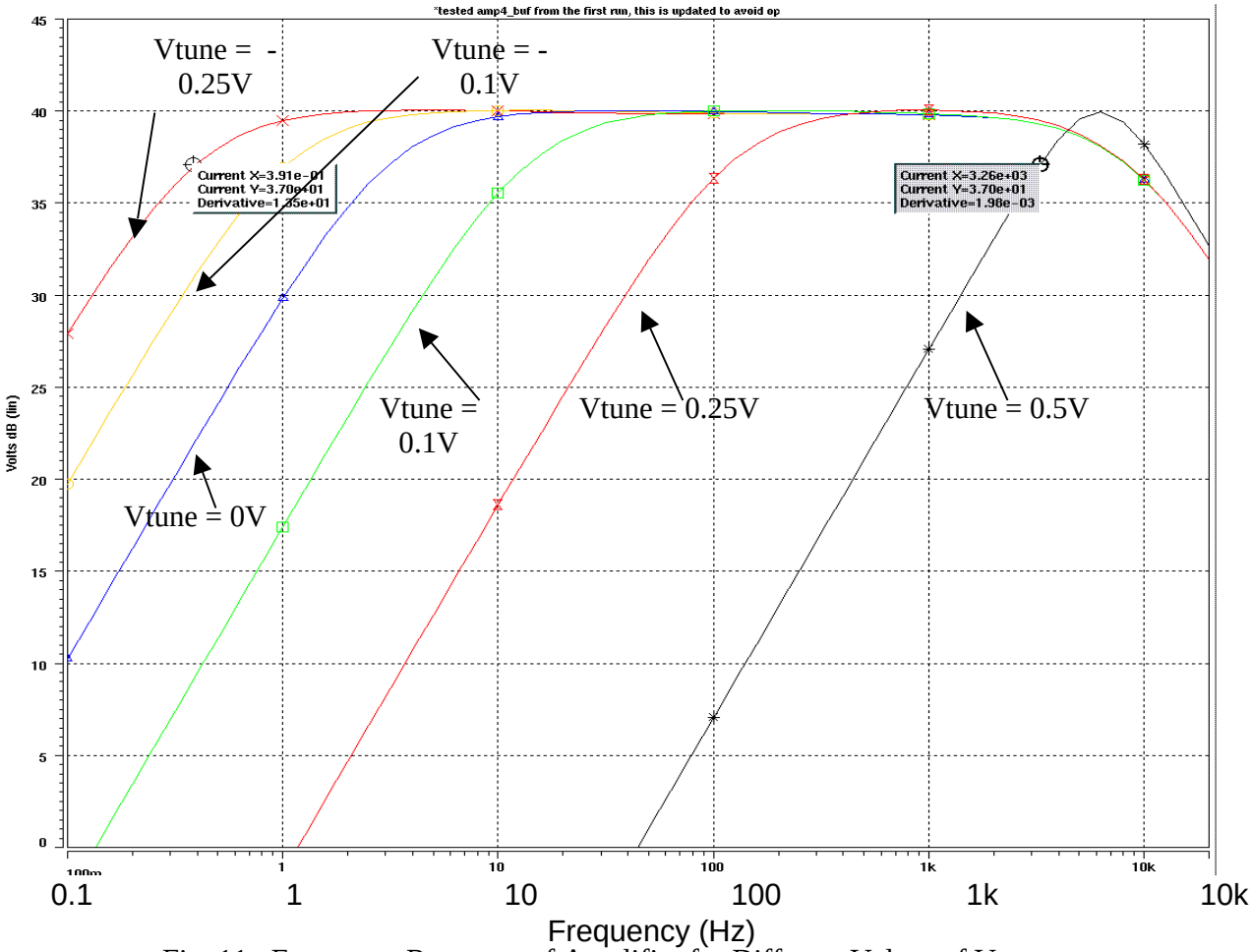

Fig. 11: Frequency Response of Amplifier for Different Values of Vtune

The design of the on-platform spike detection circuitry is on going, specifically the 5-bit A/D converter used to quantize the neural data. A block diagram of the successive approximation A/D converter is shown in Fig. 12. The input to the A/D is a sample and hold circuit, which samples the time-division multiplexed neural data in the middle of the sampling window. The track and latch comparator, which was reported in the April 2002 quarterly report, compares the sampled data to the reference voltage provided by the D/A converter. The SAR control unit, which is being designed using Verilog HDL, holds the quantized outputs and provides this data to the D/A so that the analog feedback reference voltage for the comparator can be generated. A diagram of the D/A converter is shown in Fig.10, with transistor dimensions summarized in Table 2. The D/A uses scaled current sources (M8-M22) to produce different analog output voltages. The current sources are turned on or off depending on the value of the digital feedback bits, b4-b0. Transistors M1-M7 comprise a high output impedance, wide-swing current mirror, which mirrors the appropriate ratio of the input current I_0 to both the PMOS and NMOS current sources. The nominal value of I_0 is 25μA, which will allow quantization of ±500μV action potentials with a quantization noise of 31.25μV. I_0 will be adjustable for recording spikes which have a wider/smaller signal swing with a subsequent increase/decrease in the quantization noise. Both PMOS and NMOS current sources have been used here to allow the analog output of the DAC to achieve both positive and negative values. The accuracy of the DAC will depend on how well the currents can be matched between the NMOS and PMOS devices. This puts very stringent restrictions on the maximum tolerable current mirror error and that is why the architecture consisting of transistors M1-M7 was chosen. The DAC and specifically the amplifier shown in Fig. 13, limits the speed of the ADC. The maximum settling time of the amplifier is 0.5μs and this sets the maximum bandwidth of the ADC at 400kHz. The amplifier topology chosen was adapted from (Fan You, 1996) with transistor sizes

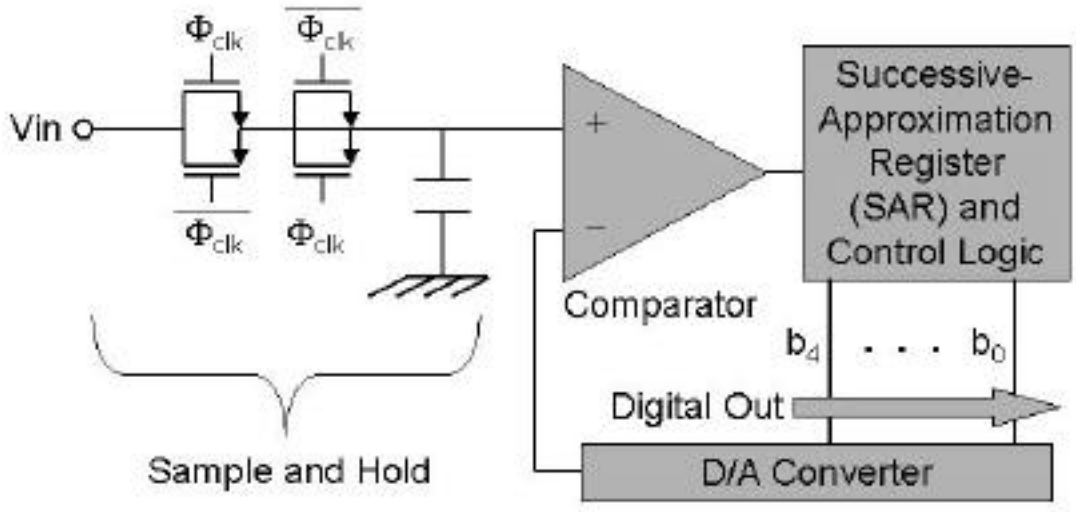

Fig. 12: Successive Approximation ADC Block Diagram

summarized in Table 3. The amplifier features a wide-swing output stage, which is necessary because standard output stages can not obtain the desired output swing from a 3V supply. The ADC consumes 330μW of power and is capable of quantizing eight time-division multiplexed channels at 5-bits of resolution.

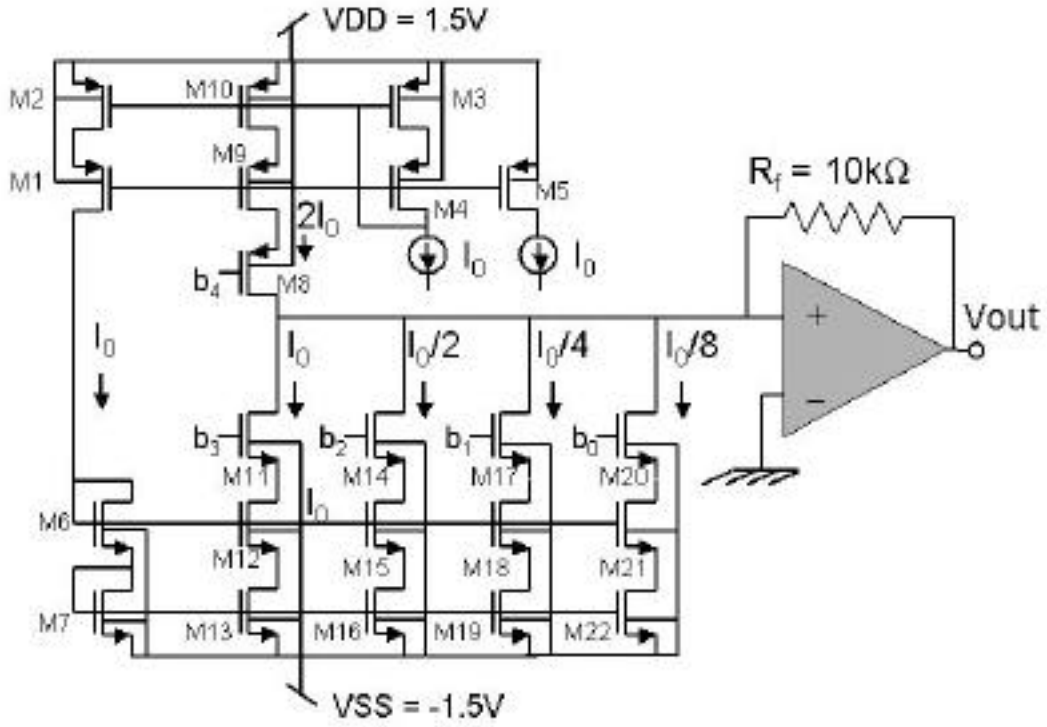

Fig. 13: Digital to Analog Converter Using Current Source Ratios

Transistors	Width (μm)	Length (μm)
M1-M4, M6, M12,	48	1.2
M5	9	1.2
M7, M13, M15	24	1.2
M8	48	0.6
M9-M10	96	1.2
M11	12	0.6
M14	6	0.6
M16, M18	12	1.2
M17	3	0.6
M19, M21	6	1.2
M20	1.5	0.6
M22	3	1.2

Table 2: Transistor Sizes for Current Source DAC

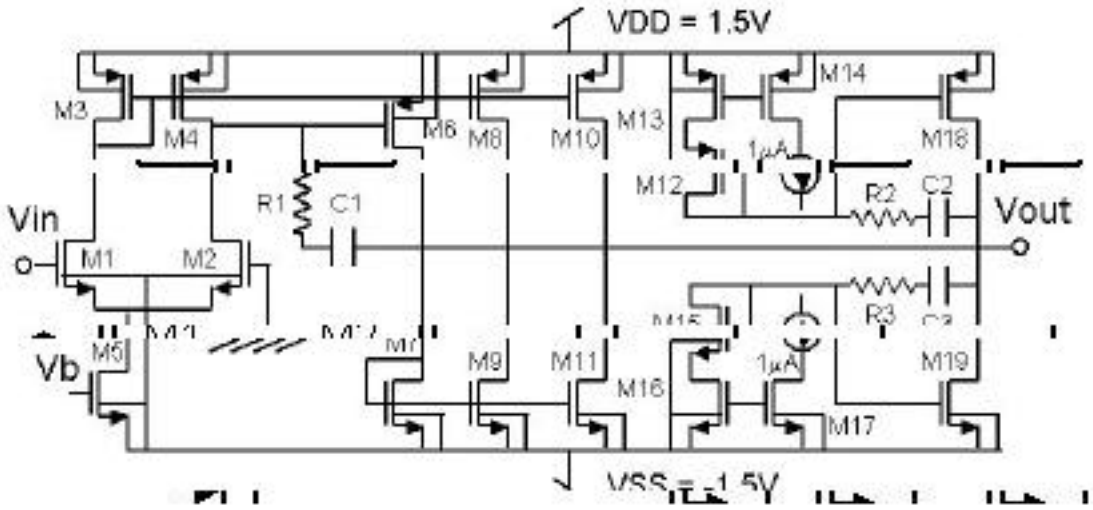

Fig. 14: Wide Output Swing Amplifier used in DAC

Device	Width (μm)	Length (μm)	Resistance (kΩ)	Capacitance (pF)
M1-M2	60	3	X	X
M3-M4, M6, M8, M10	18	3	X	X
M5	12	3	X	X
M7	13.2	3	X	X
M9, M11	12.9	3	X	X
M12-M17	3	3	X	X
M18	13.65	0.6	X	X
M19	6	0.6	X	X
C1	X	X	X	0.8
R1	X	X	5	X
C2, C3	X	X	X	3
R2, R3	X	X	30	X

Table 3: Amplifier Component Values

6. Design of a Wireless Telemetry Platform for Multichannel Microprobes

We fabricated an interface chip during the past quarter, which included front-end and an on-chip transmitter. The chip is being tested and some of measurement results are shown in this report. We also designed a hybrid charge-redistribution ADC for use in time-division multi-channel recording and logic circuit blocks for multichannel recording. Both of these are being fabricated.

Interface chip

The interface chip shown in Fig. 15 includes front-end circuitry and an on-chip transmitter. This chip is currently being tested.

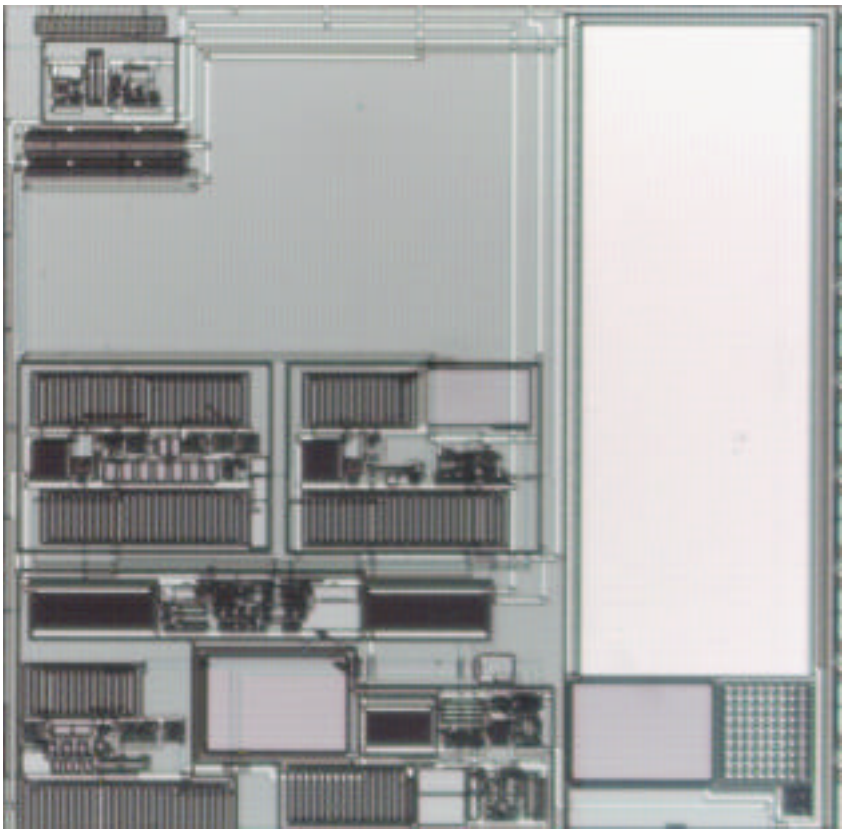

Fig. 15: The fabricated interface chip

On-chip transmitter

The measurement results for the on-chip transmitter are shown in Fig. 16. Channel 1 is the modulating data, channel 2 is the drain voltage of class-C power amplifier, and channel 3 is the induced voltage across the receiver coil. In this measurement, the carrier frequency is 49MHz and the bit rate can reach 1.6Mbps. The carrier frequency can continue to go higher if frequency control capacitors are trimmed out; higher bit rates are then expected. The power supply of the Class-C PA is 3.3V and power consumption is 1.693mW, which matches the simulation results.

Regulators

There are five regulators in this front-end circuitry, where the first stage regulator pre-stabilizes the voltage. The second stage regulators provide two 3.4V outputs (one for the digital circuitry and one for the analog circuitry) and two 1.7V outputs (one for the

digital circuitry and one for the analog circuitry). The nominal output voltage of the first stage regulator is 6V. The line regulation and load regulation are shown in Fig. 17 and Fig. 18. The line regulation is better than 3mV/V when the line voltage changes from 8V to 15V. The load regulation is better than 2mV/mA.

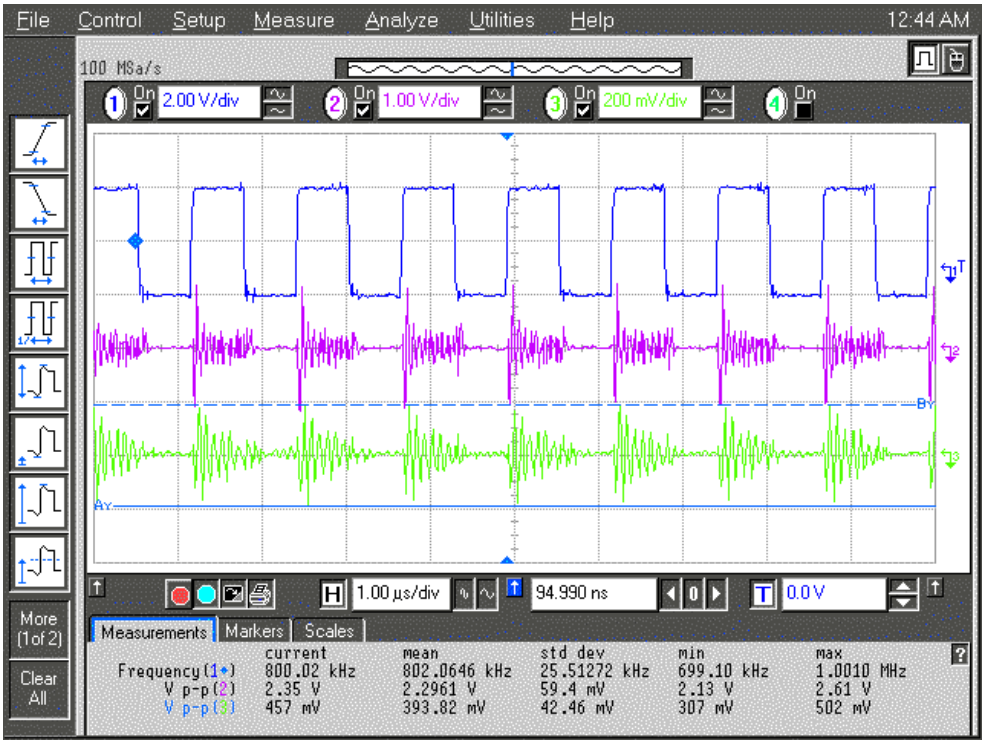

Fig. 16: Testing of an on-chip transmitter

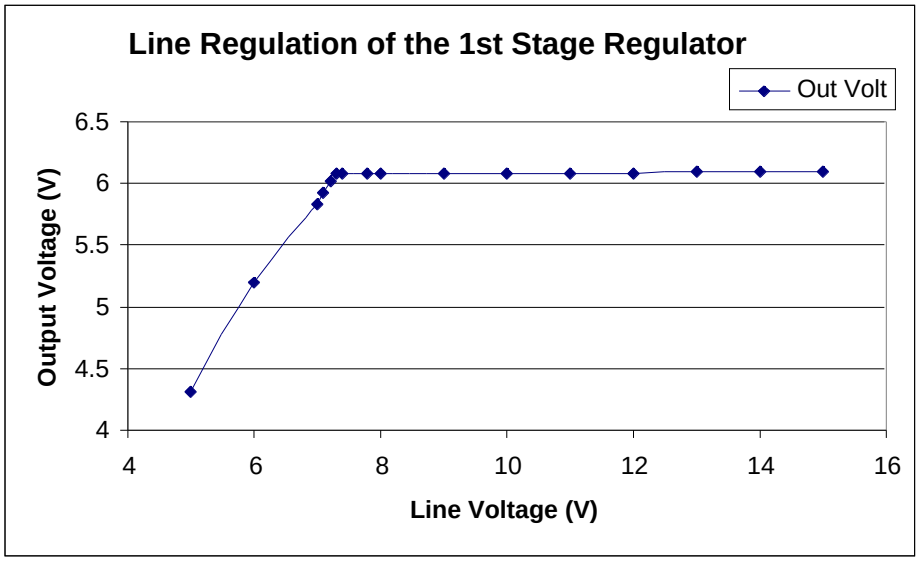

Fig. 17: Line Regulation of the 1st Stage Regulator

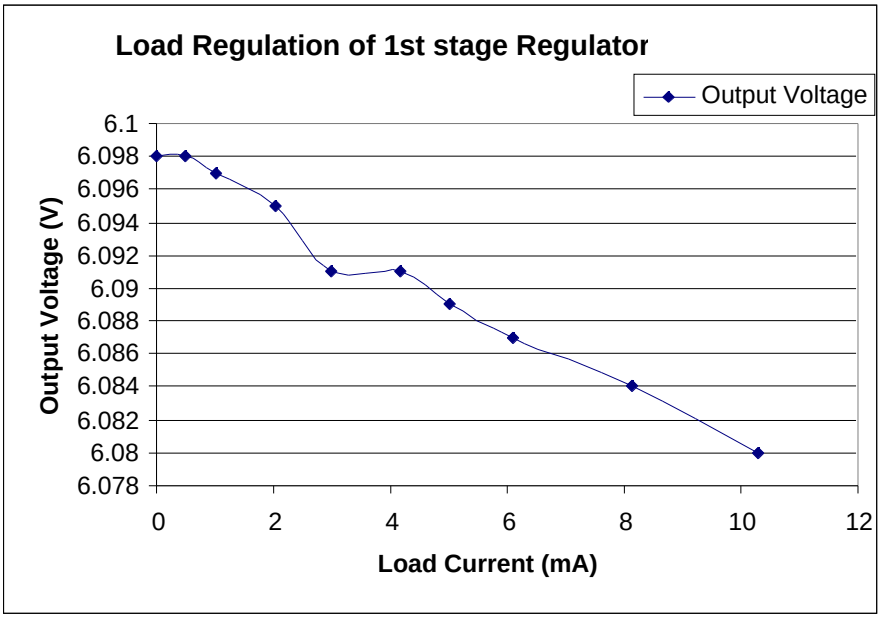

Fig. 18: Load regulation of the first stage regulator

The figures of line regulation and load regulation of 3.4V(analog, digital), 1.7V(analog, digital) regulators are shown in Attachment. And the performance is tabulated in Table 4.

Regulators	***Line Regulation***	***Load Regulation***
First stage Regulator	< 3mV/V (input 8-15V)	<3mV/mA (I_{load} 0 - 10mA)
3.4V Regulator (digital)	< 1mV/V (input 6-15V)	<8mV/mA (I_{load} 0 - 10mA)
3.4V Regulator (analog)	< 1mV/V (input 6-15V)	<2mV/mA (I_{load} 0 - 10mA)
1.7V Regulator (digital)	< 1mV/V (input 5-15V)	<10mV/mA (I_{load} 0 - 5mA)
1.7V Regulator (analog)	< 1mV/V (input 5-15V)	<0.5mV/mA(I_{load} 0 - 10mA)

Table 4. The performance of regulators

POR and Clock Regenerator

The functionality of the POR and Clock Regenerator circuits was verified, and the measurement results are shown in Fig. 19 and Fig. 20. In Fig. 19, channel 4 is the power supply of the chip and channel 2 is the output POR signal. The POR has pulse width of 290μS. In Fig. 20, channel 4 is the applied voltage across the receiver coil, which powers the interface chip, and channel 3 is the recovered clock of 4MHz.

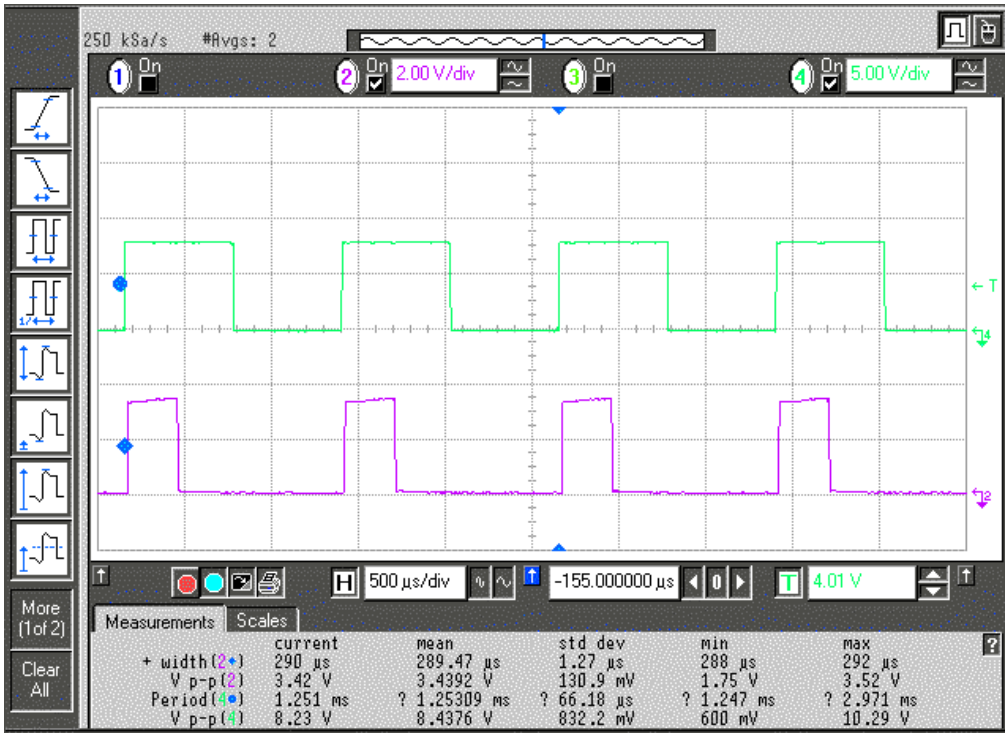

Fig. 19: The POR signal

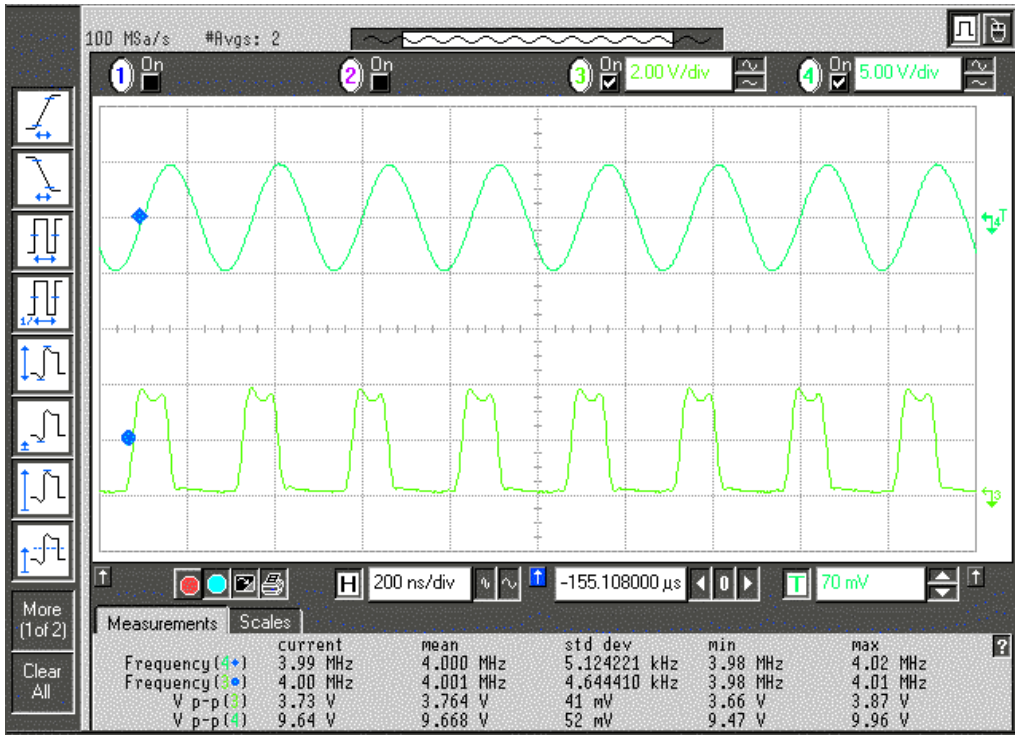

Fig. 20: Recovered Clock of 4MHz

The power consumption of the front-end was measured under a variety of voltages applied to the chip. The results are listed in Table 5. When supply voltage is 7V, the chip is fully functional and the current consumed is 68.2μA.

Supply Voltage	7V	8V	9V	10V	11V	12V	13V
Current (μA)	68.2	68.3	69.7	69.7	70.2	72.5	72.8

Table 5: Supply voltage and current consumed

A Charge Redistribution ADC

The capacitor matching tolerances limit the resolution to approximately 9-10 bits for charge-redistribution ADCs. This limit can be overcome by using hybrid approach, combining charge-redistribution capacitor array with resistor array. Fig. 21 illustrates the basic circuit diagram of a hybrid charge-redistribution A/D converter that uses a resistor array for 3-bit resolution and a capacitor array for 7-bit resolution. The operation principle of the circuit can be described as follows:

Step 1. S0 = high, S1 = high and b0-b9 = low so that the input signal can charge the capacitor array. C2 is used between two comparators to cancel the offset voltage of the 1st stage comparator.

Step 2. S0 = low, S1 = low, and start the successive approximation procedure.

Step 3. b9 is the most significant bit. Set b9 = high, the logic determines if b9 keep high or according to the output of the comparator at the next edge of the clock.

Step 4. Use the same principle as in step 3 to determine b8-b0.

Step 5. Set Ready = high and save results b0-b9 in the result register. Then go back to step 1.

The simulation results are shown in Fig. 22 and are tabulated in Table 6.

	Clock frequency	Cycle	Power consumption	Resolution
Specification	4MHz	4μs	1.27mW	10-bit

Table 6: Measurement results of for the ADC

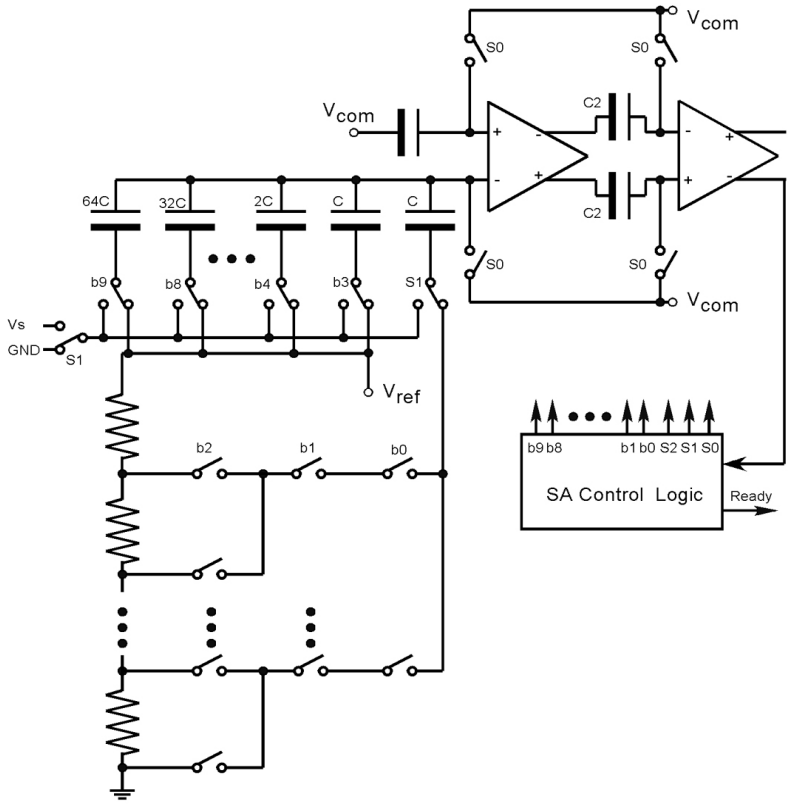

Fig. 21: A hybrid charge-redistribution ADC with 10-bit resolution

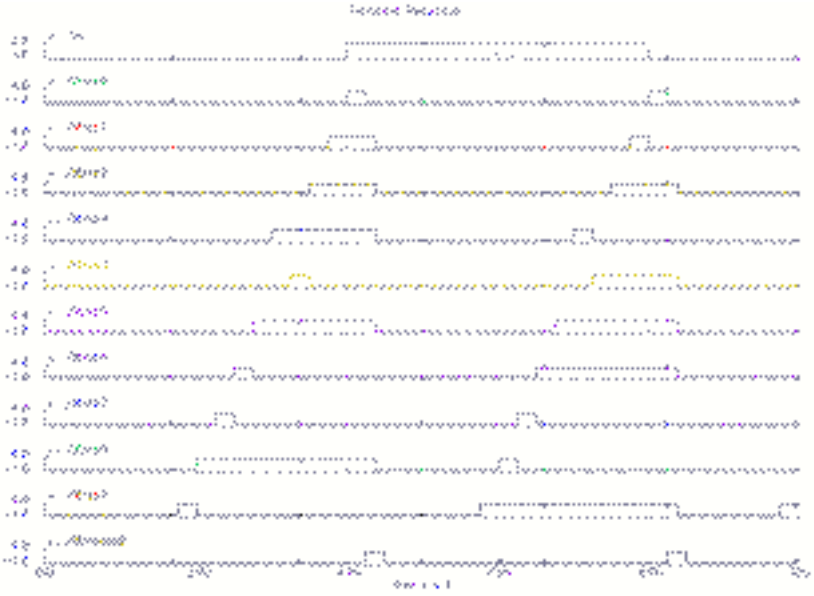

Fig. 22: Simulation results for the hybrid charge-redistribution ADC

When the input is 1V, output data is 01,0011,0110, which corresponds to 0.999V, since Vref = 3.3. When the input is 2V, output data is 10,0110,1101, which corresponds to 2.001V. This circuitry has been laid out and sent out for fabrication.

Design of the Control Logic

The control logic can be divided into four blocks with different functions. The first block is used for command decoding, and the schematic block diagram is shown in Fig. 23.

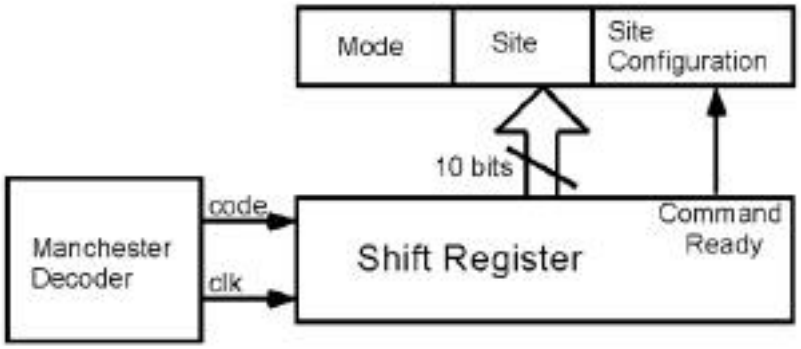

Fig. 23: command read-in circuitry

The output from ASK demodulator is fed to a Manchester decoder and the results are stored in the shift registers. When the decoded command is valid, the relevant information is then re-stored in three registers. In Fig. 23, the Mode Register (MR) determines working mode of the microsystem; the code and corresponding working mode are tabulated in Table. 7.

Code	00	01	10	11
Working mode	One channel recording. Use hybrid charge redistri-bution ADC	Time-division multichannel recording. Use hybrid charge-redistribution ADC	High resolution one channel recording. Use Sigma-Delta modulator	Stand-by

Table 7: Working modes of the microsystem

The Site Configuration Register (SCR) and Site Register (SR) are used in probe control and channel selection. There will be 64 channels on the implant probe, among which one site configuration (including 8 channels) will be selected for recording according to the SCR (Site Configuration Register). If the working mode of the microsystem is set up as multichannel recording, these eight channels will be sampled in turn and recorded; if the mode of the microsystem is set to single-channel recording, one channel will be chosen from these eight channels according to SR (Site Register). Simulation results for the command read-in logic circuit are shown in Fig. 24, where signal /M_in is fed from ASK demodulator to the Manchester decoder, whose output includes clock (/M_clk) and code (/M_code). If the input is a valid series of command, the signal /command becomes high, and data in shift registers are latched into MR, SCR and SR. The simulation results match the expectation.

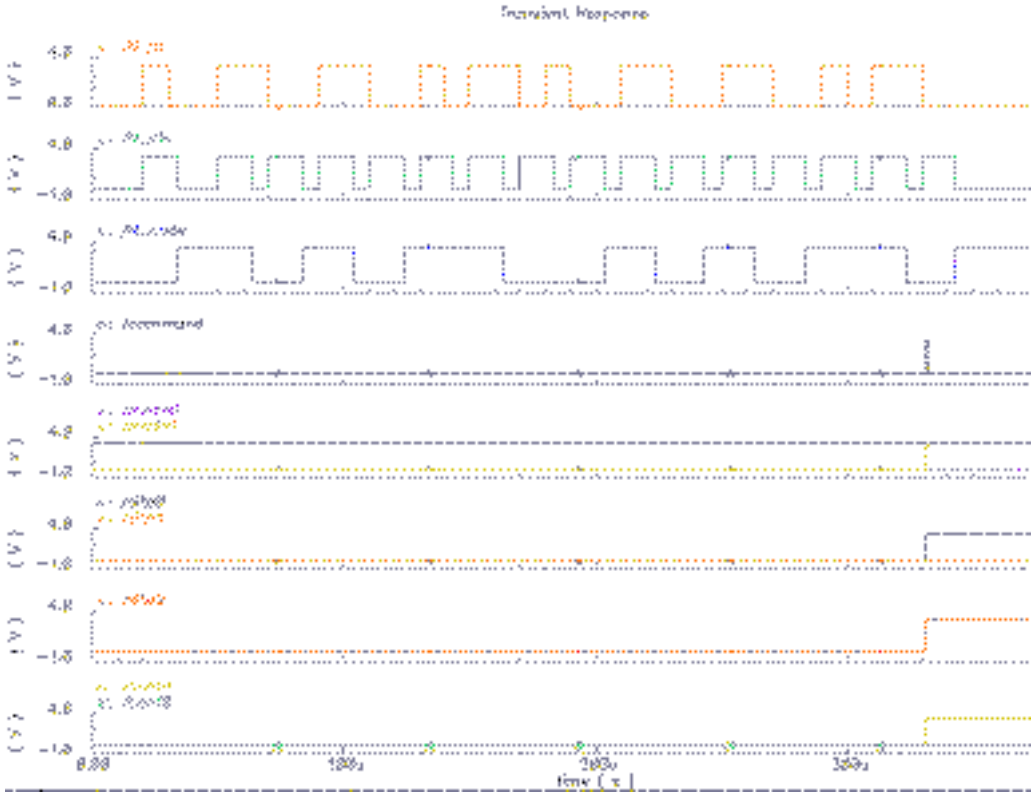

Fig. 24: Simulation for command read-in circuitry

The second block shown in Fig. 25 is used to control the probe. It sends clock and control signals to the probe in order to choose channels of interest for recording. The simulation results are shown in Fig. 26. The outputs of the probe control logic circuitry are /Site_RST, /Site_clk, /Conf_Addr and /Conf_mode, which are fed to the active probe. Control logic has been verified by Troy Ollson, who designed the circuitry on probe. The third logic block is a Manchester encoder used to encode the digital output of the ADC for data transmission. Its block diagram is shown in Fig. 27 and the simulation results are shown in Fig. 28.

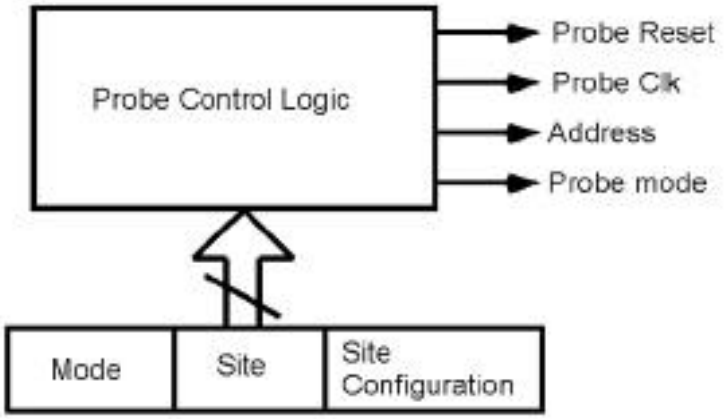

Fig. 25: Block diagram of the probe control logic

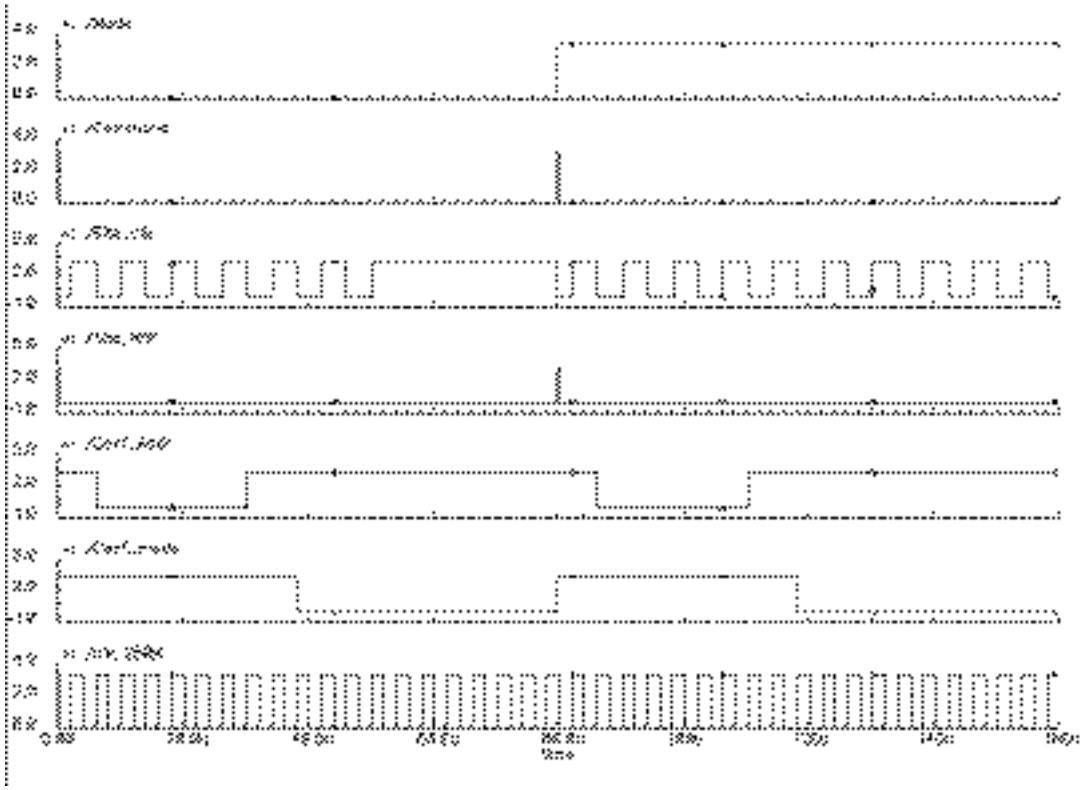

Fig. 26: Simulation results for the probe control logic

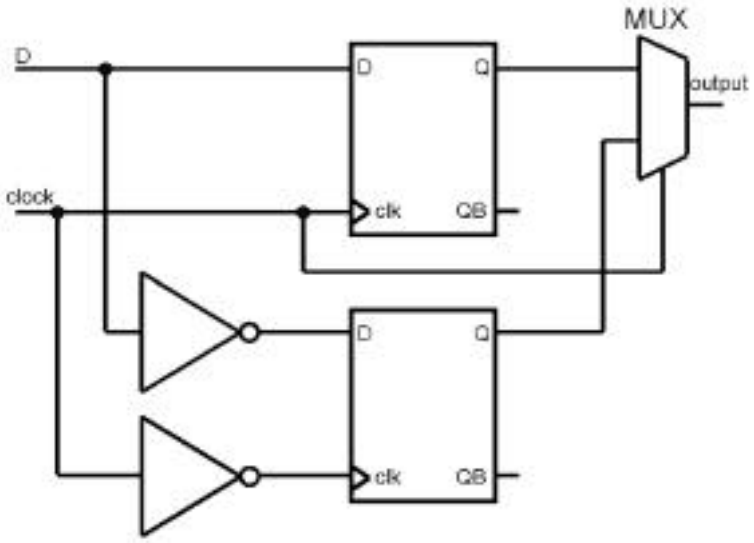

Fig. 27: The Manchester encoder

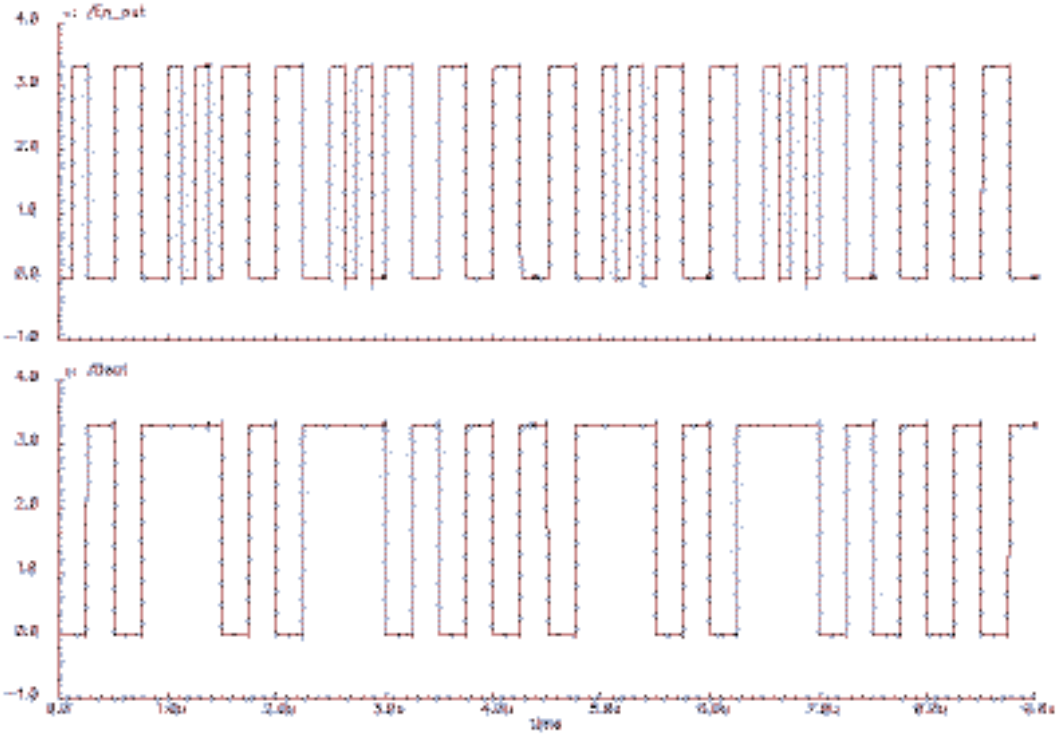

Fig. 28: Simulation results for the Manchester encoder

An additional block is needed between Manchester encoder and charge-redistribution ADC, shown in Fig. 29; this logic has been verified when simulated together with ADC. All of the logic blocks are now ready for fabrication.

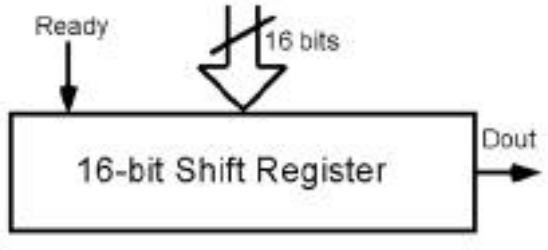

Fig. 29: Parallel-in-Serial-out shift register

7. Conclusions

During the past quarter, we have continued to distribute passive probes built with technology developed under these contracts to investigators nationwide. Nearly 5000 probes have now been provided, resulting in over 180 publications and presentations. A new mask set is now in preparation for fabrication this fall.

The first soak tests of active probes also began last quarter. The test vehicle was a 32-site front-end selected and buffered probe that also contained a number of test structures, including test transistors. The probe circuitry was encapsulated with LTO, which in some cases was covered by sputtered or electroplated gold shields. For probes operated at body temperature, the primary change noted was an increase in gate current for the test transistors; for probes soaked at 70°C, the bonding pads failed early in the tests. There was no observed degradation of the interconnect on the probes, however. At this point it is not known where the shift in the gate currents is an on-chip change or whether it is associated with the leads from these devices. We suspect the latter. In a second series of tests with an improved lead structure, the probes have been functioning for over a week with no noted changes at body temperature. Probes with integrated ribbon cables will be tested during the coming quarter.

We have now performed additional tests on the capacitively-coupled amplifiers developed for the probes, correcting earlier measurements of their associated noise. The amplifiers have an input-referred noise of 16.6μVrms (10Hz – 10kHz). For the site, input selector, and amplifier together, the noise is 19.2μVrms. We have iterated the amplifier design to reduce its noise to 7.2μVrms. The amplifiers provide a gain of 38.2dB with a power-supply-rejection-ratio of 50.5dB. The output offset voltage is –45mV, which is adequate for the succeeding multiplexers. On-platform spike detection circuitry is being designed with a 5b successive approximation converter. The ADC has a maximum bandwidth of 400kHz and dissipates 330μV from ±1.5V supplies.

We are also in the final stages of designing a wireless interface to the recording probes. The chip being characterized includes all of the front-end circuitry for the probes along with the on-chip transmitter. This transmitter is presently being characterized at a carrier frequency of 49MHz, where it allows bit rates of 1.6Mbps and dissipates 1.7mW from 3.3V. The on-chip voltage regulators produce 1.7V and 3.4V outputs with line regulation better than 3mV/V and load regulation better than 2mV/mA. The power-on-reset circuitry produces a reset pulse width of 290µsec. The front-end circuitry is fully functional with an overall dissipation of about 480µW from 7V. A 10b ADC is being designed for use with analog output probes. It dissipates 1.27mW at a cycle time of 4µsec. The front-end control logic verifies the input commands received using a Manchester encoder and formats the received commands/data for use by the probes. The last of these circuit blocks are now ready for fabrication. We hope to operate the entire probe system wirelessly by the end of the year.

Attachment

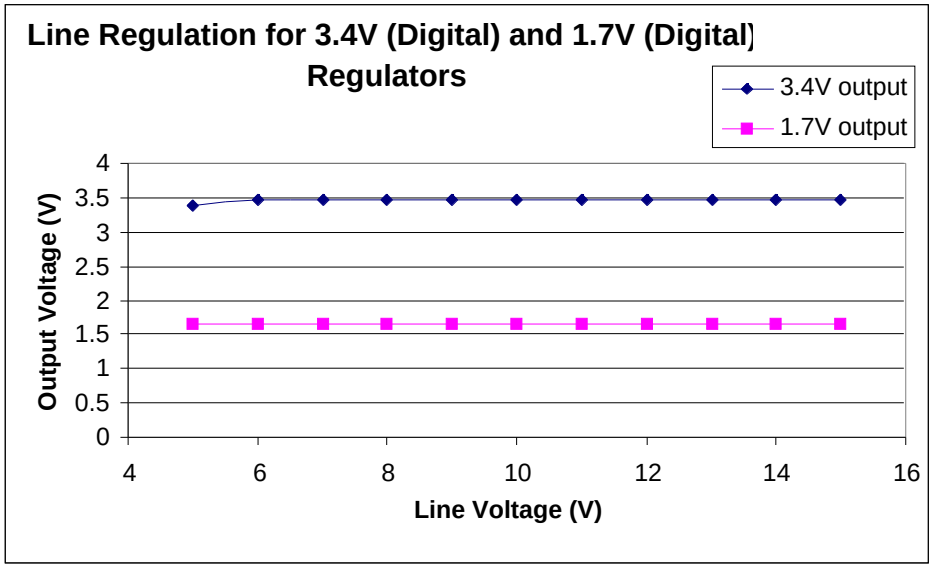

Fig. A-1: Line Regulation for the 3.4V(Digital) and 1.7V(Digital) Regulators

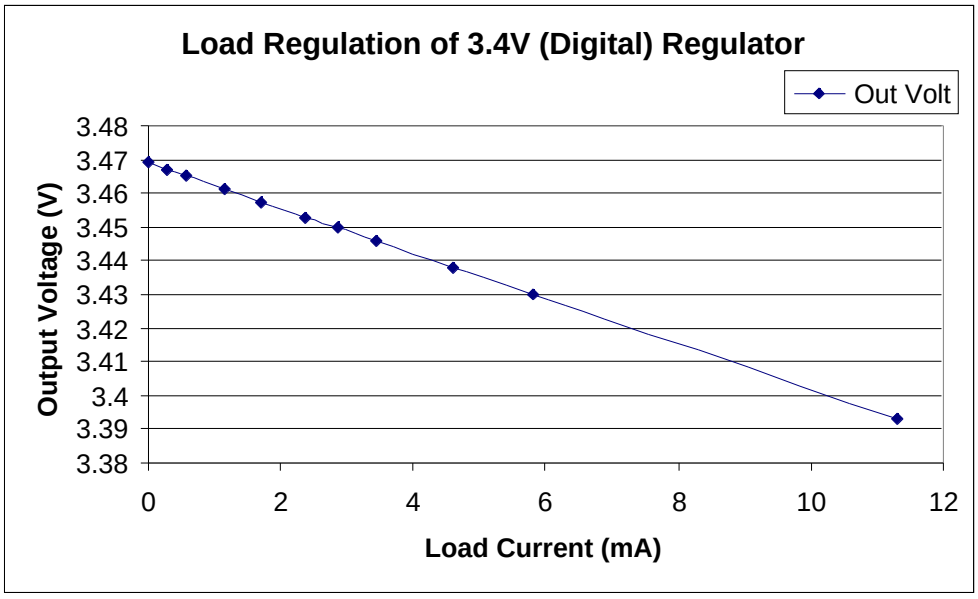

Fig. A-2: Load Regulation for the 3.4V(Digital) Regulator

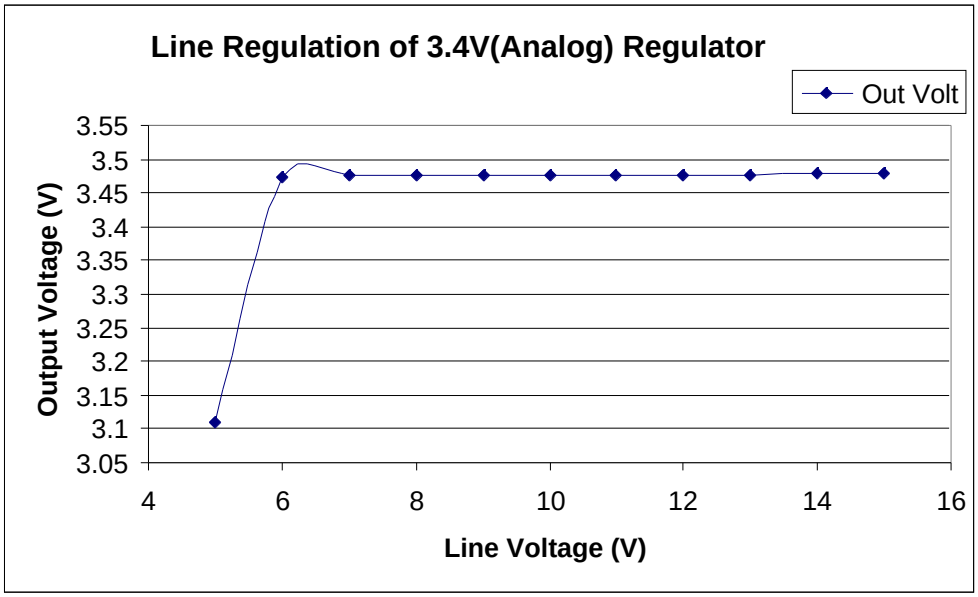

Fig. A-3: Line Regulation for the 3.4V(Analog) Regulator

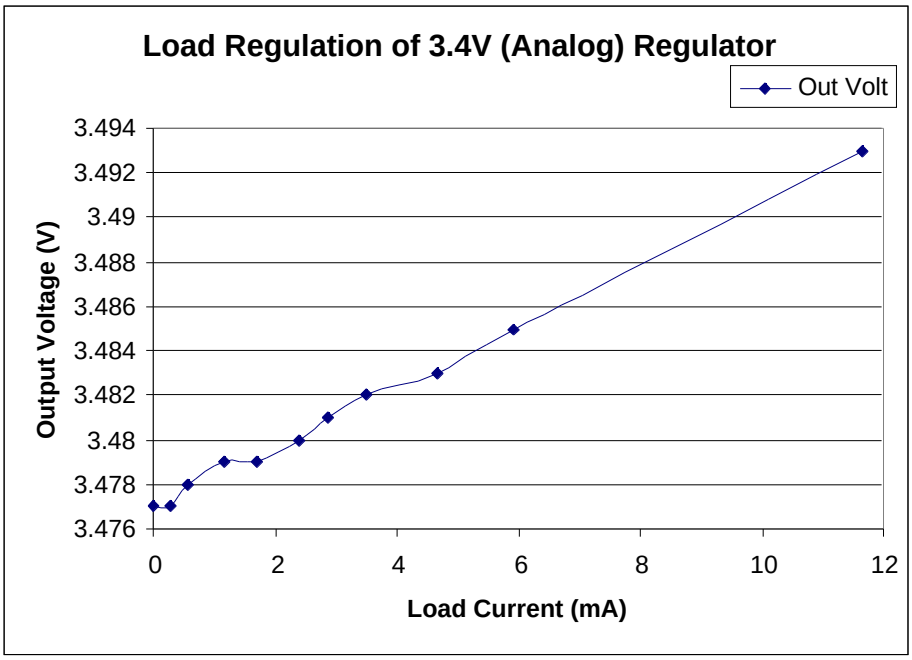

Fig. A-4: Load Regulation for the 3.4V(Analog) Regulator

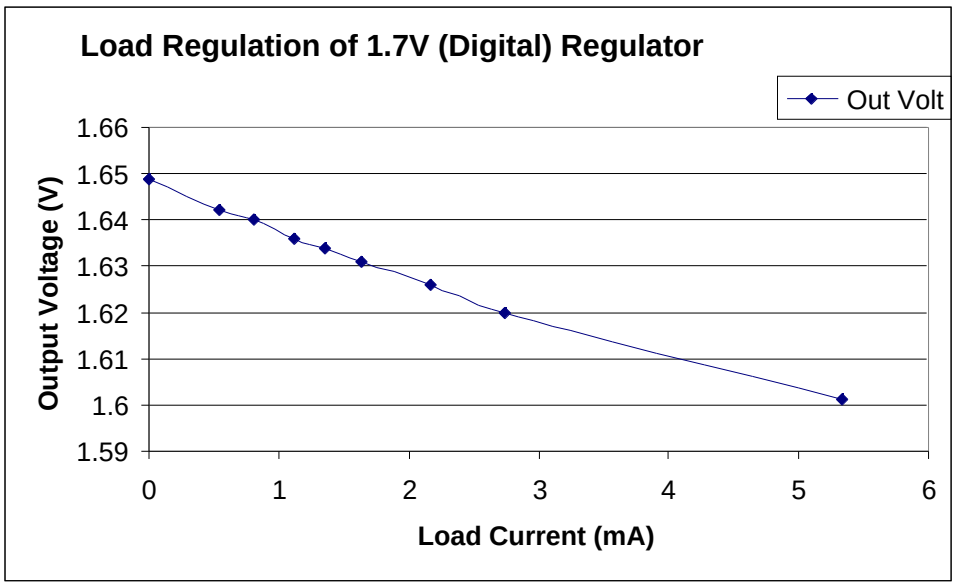

Fig. A-5: Load Regulation for the 1.7V(Digital) Regulator

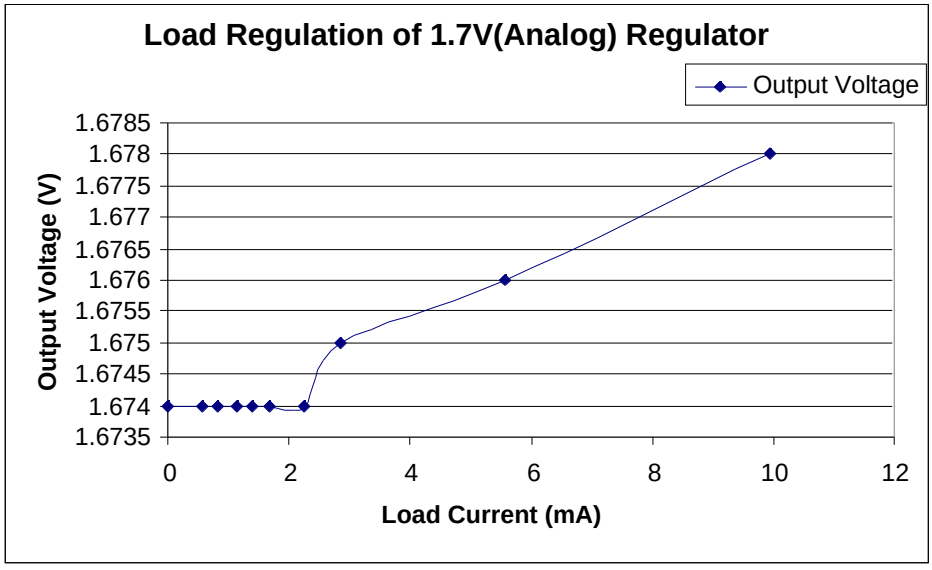

Fig. A-6: Load Regulation for the 1.7V (Analog) Regulator

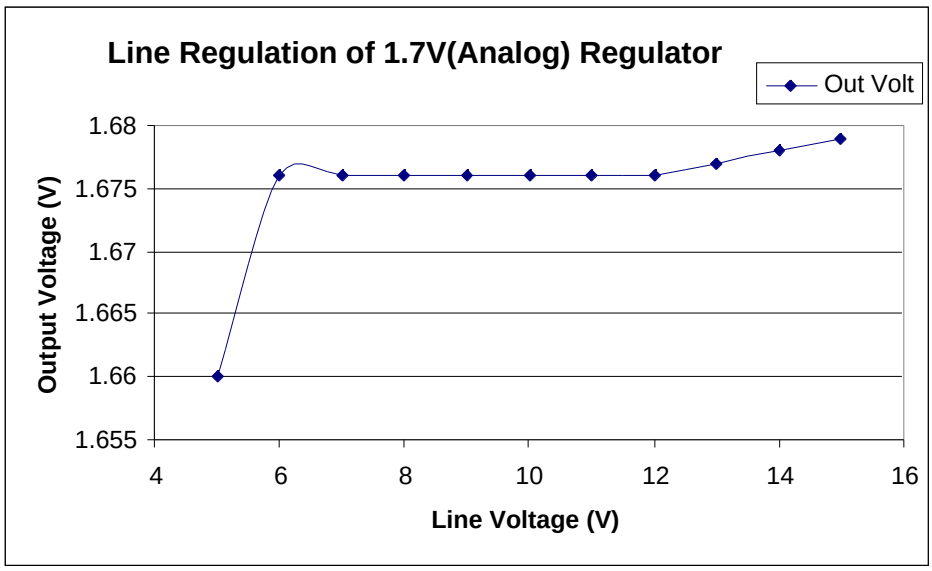

Fig. A-7: Line Regulation for the 1.7V(Analog) Regulator